What is claimed:

SUB C1

1. A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a storage node of the cell capacitor and a lower electrode of the capacitor element;

(b) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(c) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

2. A method for manufacturing a semiconductor device according to claim 1, further comprising, before the step (a), the step of simultaneously forming

a word line that is a component of the DRAM and

a connection layer that is located in a common layer of the word line and that electrically connects the lower electrode to another element in the semiconductor device.

3. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

4. A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

5. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

6. A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried simultaneously with step (c), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

7. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) carried out simultaneously with step (c), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

8. A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

9. A semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the semiconductor device comprising:

an interlayer dielectric layer and an embedded connection layer,

wherein the interlayer dielectric layer is located between the semiconductor substrate and the capacitor element,

the embedded connection layer is used to electrically connect a lower electrode of the capacitor element to another semiconductor element,

the embedded connection layer is located at a connection hole formed in the interlayer dielectric layer, and

one end section of the embedded connection layer connects to the lower electrode at a bottom surface of the lower electrode.

10. A semiconductor device according to claim 9, further comprising

a connection layer connected to a second end section of the embedded connection layer,

wherein the connection layer is used to electrically connect the lower electrode to another semiconductor element, and

the connection layer is located in a common layer of a word line that is a component of the DRAM.

11. A semiconductor device according to claim 10, further comprising

an additional capacitor element,

wherein the additional capacitor element is located in the analog element region, and

the capacitor element and the additional capacitor element are serially connected to each other by the embedded connection layer and the connection layer.

12. A semiconductor device according to claim 9 further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

an impurity concentration of the first resistance element is higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

13. A semiconductor device according to claim 9, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

the first resistance element includes a silicide layer so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

14. A semiconductor device according to claim 9, wherein a thickness of a dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of the cell capacitor.

15. A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the cell capacitor and a lower electrode of the capacitor element;

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the cell capacitor and a dielectric layer region of the capacitor element; and

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the cell capacitor and an upper electrode of the capacitor element.

16. A method according to claim 15, further comprising, prior to forming the storage node of the cell capacitor and the lower electrode of the capacitor element,

form an additional conducing layer and etching the additional conducting layer to form a word line that is a component of the DRAM and to form a connection layer that is located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device.

17. A method for manufacturing a semiconductor device according to claim 15, wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region, and wherein the first resistance element and second resistance element are formed with a resistance value of the first resistance element being lower than that of the second resistance element.

18. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region, wherein the step (d) is carried out simultaneously with step (c), and wherein an amount of impurity ion-implanted in a region where the first resistance element is to be formed is greater than an amount of impurity ion-implanted in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.